DETAILED ACTION

1. This office action is in response to the reply filed on 11/19/2009.

2. Claims 1 and 3-13 are pending in the application and have been examined.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1, 3, 5 and 9-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stolan (U.S. Patent 5,864,663) in view of Juzswik (U.S. Patent 4,698,748).

6. Regarding claims 1, 5 and 9, Stolan discloses a method of monitoring the operation of at least one microcontroller unit that is intended for at least one application and is associated with a system, by means of at least one base chip, particularly a system base chip [col. 1, lines 11-16; a circuit monitors a microprocessor], characterized in that:

a reset of the microcontroller unit is caused if a reset condition is detected, wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip [col. 2, line 66 – col. 3, line 4] and the reset of the microcontroller unit is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip [col. 2, line 66 – col. 3, line 4; the system selects either an overflow condition or an external reset; the external reset system constitutes part of the "special sequence"; by selecting the external reset and then detecting that the external reset is set, the system is "checking" whether the special sequence has been successfully applied]; and

a special mode of operation, particularly a flash mode of the base chip, can be activated once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation, by allowing access to at least one monitoring module that is associated with the base chip to take place in a manner which is simplified in comparison with the normal mode of operation of the microcontroller unit [col. 2, lines 41-45; col. 2, line 66 – col. 3, line 4; col. 5, lines 5-16; a programmable reset can be used in place of a watchdog timer reset].

Stolan does not explicitly disclose the steps of supplying a permanent energy supply from a battery unit to the monitoring module; and switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit. However, Juzswik discloses using this technique [col. 2, line 32 – col. 3, line 4] for the purpose of reducing power consumption in a system having a microprocessor and a watchdog timer. Such operation would therefore have been obvious in the system of Stolan.

7. Regarding claim 3, Stolan discloses a method as claimed in claim 1, characterized in that: during the special mode of operation, use is made of a special trigger code or a special trigger signal for the monitoring module that is different from the normal mode of operation [col. 2, lines 41-45; col. 2, line 66 – col. 3, line 4; col. 5, lines 5-16; a programmable reset can be used in place of a watchdog timer reset]; and a fresh reset of the microcontroller unit is caused by the normal trigger code or the normal trigger signal, to enable the special mode to be exited again [col. 5, lines 5-16; a signal determines which type of reset may occur].

8. Regarding claims 10-13, Stolan in view of Juzswik discloses that the microprocessor is intended for the electronics of motor vehicles [Juzswik, col. 1, lines 18-23].

9. **Claims 4 and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stolan in view of Juzswik as applied to claims 1 and 5 above, and further in view of Ubicom (*Ubicom Product Report – IP2022 Internet Processor*).

10. Regarding claims 4 and 6, Stolan discloses a method as claimed in claim 1, characterized in that: a distinction can be made between reset events that differ in relation to the operation of the microcontroller unit [col. 5, lines 5-16; a signal determines which type of reset may occur]. Stolan does not explicitly disclose that these different reset events are suitably logged and made known in at least one register unit by means of different register entries. However, as shown by Ubicom [page 22, sections 3.6.2, 3.6.3], such operation is common in processing systems because it is advantageous to know the cause of a reset in order to perform specific processing operations associated with that type of reset. It therefore would have been obvious to perform such operation in the system of Stolan.

11. Regarding claim 7, Stolan in view of Ubicom discloses a base chip as claimed in claim 6, characterized in that: the monitoring module is triggerable in particular by means of at least one interface unit [Stolan, col. 2, lines 41-45; col. 2, line 66 – col. 3, line 4; col. 5, lines 5-16; an interface unit causes a reset]; and/or to distinguish between the particular accesses to the monitoring module, different reset events can be marked by different trigger codes or trigger signals [Stolan, col. 2, lines 41-45; col. 2, line 66 – col. 3, line 4; col. 5, lines 5-16; different signals indicated different types of resets].

12. Regarding claim 8, Stolan in view of Ubicom discloses a base chip as claimed in claim 7, characterized in that there is provided between the monitoring module and the microcontroller unit at least one signal line for transmitting at least one trigger code or trigger signal that differs from the normal mode of operation of the microcontroller unit [Stolan, col. 2, lines 41-45; col. 2, line 66 – col. 3, line 4; col. 5, lines 5-16; a programmable reset can be used in place of a watchdog timer reset].

Double Patenting

13. The double patenting rejections made in the previous office action are held in abeyance until a time at which patentable subject matter is determined.

Response to Arguments

14. Applicant's arguments filed 11/19/2009 have been fully considered but they are not persuasive. Applicant alleges that the application of the teachings of Juzswik to the system of

Stolan changes the principle operation of Stolan. This argument is not persuasive for at least two reasons.

First, the teachings of Juzswik merely present an alternative method for monitoring the operation of a microprocessor. Applicant argues that Stolan checks a counter every millisecond and that the application of Juzswik to Stolan would prevent this check from occurring. However, that is the purpose of using the Juzswik reference: to modify the Stolan reference. The combination of the two references results in a different monitoring system that saves power (but does not check a counter every second). Applicant's argument appears to be that any modification made to a primary reference that changes its operation constitutes a change to its principle of operation. If that were the case, no two references could ever be properly combined.

Second, the specific functionality of Stolan [the checking of a counter every millisecond] that applicant cites as the "principle of operation" is not being relied upon for the rejection. Thus, applicant's argument isn't even relevant to the rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey Faherty whose telephone number is (571)270-1319. The examiner can normally be reached on weekdays between 7:00 and 4:30, with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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